
SARANCE TECHNOLOGIES

Intellectual Property Product Brief Binary CAM CORE

INTRODUCTION

A Content Addressable Memory (CAM) is an array of data words that can each be simultaneously compared to a search key to identify a match between the key and a word in the array. A successful comparison returns a match indicator as well as the position of the matching data word in the CAM array. CAMs are used in various telecommunications applications that require a fast match on some portion of a packet header.

Sarance Technologies has developed a configurable CAM core that can be used to implement small CAM tables in an FPGA. The CAM core has configurable bit width and depth and operates at search speeds of up to 200 MHz.

The CAM core outlined in this brief is a true implementation of a CAM. That is, it is implemented such that each entry is truly searched simultaneously. When implemented in an FPGA, this works well for small tables, but does not scale well for large CAM tables. For large tables an algorithmic approach, while much more complicated, is a better approach. Sarance Technologies offers a number of algorithmic cores that implement the function of a CAM, but use a much smaller resource and power footprint than an equivalent 'true' CAM implementation does. Please refer to the exact match and LPM product briefs for more details on Sarance's algorithmic search engines.

CAM CORE ARCHITECTURE

The CAM Core architecture consists of an array of CAM cells that are simultaneously compared to an input search key. Each matching cell generates a 'hit' flag that is fed into a priority encoder. The priority encoder then returns the index of the matching CAM cell, along with the match flag, to the user. In the event that multiple entries within the table generate a match condition, the highest priority index will be returned. The default setting for determining the highest priority is based on the CAM cell index. The lower the index, the higher the priority.

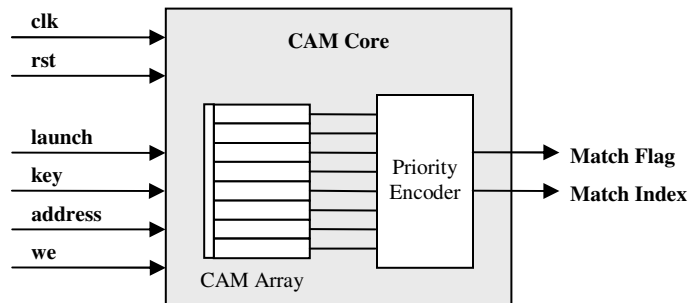


Figure 1. CAM Core Block Diagram

KEY FEATURES

- 200 MHz exact match search operation
- Configurable key width of 8 to 80 bits
- Configurable table depth of 32 to 1K entries
- Single cycle search latency
- Inline management interface

CAM CORE INTERFACE

The following table details the interface to the CAM core.

Signal	Type	Width	Description
clk	Input	1	The clock input to the CAM core. The core will perform searches at the frequency of the clock input.
rst	Input	1	Asynchronous active high reset
launch	Input	1	Launch Input, active high. When active, the CAM core will perform a search operation on the next rising edge of <i>clk</i> . Note that <i>we</i> and <i>launch</i> cannot be active on the same clock cycle.
key	Input	8-80	The search key. When <i>launch</i> is active, the CAM core will perform a search on <i>key</i> .
address	Input	5-10	On a write operation, the contents of <i>key</i> will be written to the CAM cell identified by the input on the <i>address</i> line.
we	Input	1	Write enable signal, active high. When active, the CAM cell identified by <i>address</i> will have the content of <i>key</i> written to it. Note that <i>we</i> and <i>launch</i> cannot be active on the same clock cycle.
match	Output	1	Match flag, active high. When active, this flag indicates that a CAM search operation has resulted in a successful match. The flag is valid one cycle after a search operation has been launched.
match index	Output	5-10	When the match flag is asserted, match index will identify the CAM cell that matched the input search key.

IMPLEMENTATION

The CAM core has been implemented using generic Register Transfer Level (RTL) Verilog source code, and can be targeted at either FPGA's or ASICs. FPGA netlists are available for Altera StratixII FPGAs. The following table outlines resource utilization in a StratixII FPGA for some specific CAM core configurations.

CAM Core Sample Resource Utilization for a StratixII FPGA

Configuration	Total ALUTs	Total Registers
256 deep x 24b wide	7312	6400
32 deep x 24b wide	911	800

AVAILABILITY

The CAM Core is available for licensing for implementation in an FPGA or ASIC, and can be purchased as either a targeted FPGA netlist or as generic Register Transfer Level (RTL) Verilog source code. Both options come with a test bench and users manual.

Sarance Technologies also provides a broad range of FPGA design services to help customize the CAM Core IP to a specific requirement or to accelerate time to market of complex FPGA designs.

For more details on licensing or customizing Sarance IP to a specific requirement, or on general design services, please contact Sarance Technologies Inc at customers@sarance.com.

Tel: 613-792-4050
customers@sarance.com

Sarance Technologies Inc.
www.sarance.com

880 Lady Ellen Place
Ottawa ON
K1Z 5L9