

INTRODUCTION

Interlaken is a scalable chip-to-chip interconnect protocol designed to enable transmission speeds from 10Gbps to 100Gbps and beyond. Using the latest SERDES technology and a flexible protocol layer, Interlaken minimizes the pin and power overhead of chip-to-chip interconnect and provides a scalable solution that can be used throughout an entire system. In addition, Interlaken uses two levels of CRC checking and data scrambler to ensure data integrity and link robustness.

Sarance's Interlaken IP Core (IIPC) is delivered as a netlist targeted at a specific FPGA architecture. The IIPC is compliant with the Interlaken Protocol Definition, Revision 1.1, and offers system designers with a risk-free and quick path for adopting Interlaken as their chip-to-chip interconnect protocol.

BLOCK DIAGRAM

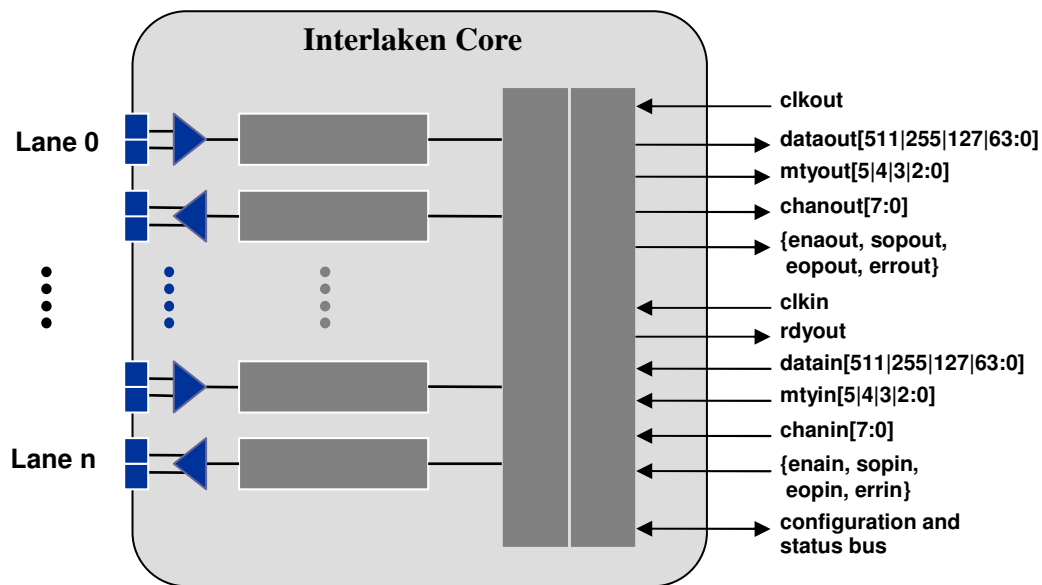


Figure 1. Block Diagram

CORE FEATURES

- Compliant with the Interlaken Protocol Definition, Revision 1.1
- Support for up to 6.375 Gbps serial data rate
- Programmable BurstMax, BurstMin, BurstShort and MetaFrameSize parameters
- Data striping and de-striping across 1 to 20 lanes (limited by FPGA I/O resources)
- 64/67 encoding and decoding
- Automatic word and lane alignment
- Self-synchronizing data scrambler
- Configurable internal data bus width of 64, 128, 256 or 512bits
- CRC24 generation and checking for burst data integrity
- CRC32 generation and checking for lane data integrity
- Data scrambling and disparity tracking to minimize baseline wander and maintain DC balance
- Support for Synchronization, Scrambler State, Diagnostic, and Skip Word Block Types
- Programmable Rate Limiting circuitry
- Error condition detection and recovery
- Channel-level and link-level flow control mechanism
- Full error checking and recovery as defined by Interlaken specification

PROTOCOL FEATURES

Interlaken is a very flexible and customizable protocol. The following protocol features are offered in Sarance’s standard cores and offer compliance with the Interlaken Protocol Definition, Revision 1.1. Certain features, such as number of logical channels and flow control, can be modified depending on the application; please contact Sarance Technologies for more information.

- Support for 256 different logical channels
- Segment-mode and Packet-mode transmission format
- Segment-mode and Packet-mode receive format
- BurstMax size can be programmed up to 256 bytes
- Support for BurstShort requirement of 32 bytes
- Optional Schedule Enhancement add-on module including support for programmable BurstMin parameter
- In-band flow control
- Support for link-level flow control
- Flow control mechanism supports stopping packets in mid-stream
- Rate matching with granularity of 1 Gbps
- Max Frame Length programmable between 128 to 8K words
- Support for status messaging

CONFIGURATION AND RESOURCE UTILIZATION

Table 1 shows the configuration and resource utilization for each of the standard core offerings implemented in the Altera® Stratix® II GX FPGA family. Note that LUT utilization is rounded up as the exact count depends on the particular synthesis setting used when compiling the core.

Table 1. Stratix II GX Resource Utilization

Bandwidth	Configuration	LUTs	Memory Bits	Core Clock Frequency
12.75 Gpbs	2 lanes @ 6.375 Gbps	5000	25K	200 MHz
25.5 Gbps	4 lanes @ 6.375 Gbps	10000	45K	200 MHz
51 Gbps	8 lanes @ 6.375 Gbps	25000	60K	200 MHz
76.5	12 lanes @ 6.375 Gbps	38000	241K	200 MHz

AVAILABILITY

The Interlaken FPGA Core is available for implementation in FPGAs as an embedded IP block, and can be purchased as a targeted FPGA netlist. Deliverables include a sample test bench and detailed users manual.

The IIPC is also available for ASIC based designs. Contact Sarance Technologies for more information.

For more details on licensing or customizing the core to a specific requirement, or on general design services, please contact Sarance Technologies Inc at customers@sarance.com.

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