

# How to Design an Interlaken <-> SPI-4.2 Bridge

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## Introduction

Future of networking is about higher bandwidth and lower power. More and more applications, such as video, continue to drive the bandwidth demand placed on networking equipment. At the same time, networking equipment must deliver the higher bandwidth without dramatic increase in power consumption. Every aspect of a system is affected by these requirements and, specifically for chip-to-chip interconnect technology; traditional solutions fail to meet these demands.

Interlaken is a relatively new chip-to-chip interconnect technology developed by Cisco Systems and Cortina Systems to help pave the way for the future of networking. Interlaken is based on low-power high-speed serial links and it is designed to be easily scalable to any bandwidth. It can meet the demand of today's 20 Gbps and tomorrow's 100 Gbps system by providing the following features:

- Low pin-count, low-power serial connectivity
- Channelized protocol
- Robust error checking and management
- Low protocol overhead

As more and more application specific standard products (ASSPs) are manufactured with Interlaken interfaces, there is a need for bridging devices to connect these new ASSPs to legacy devices with different interfaces. Figure 1 shows the block diagram of a typical networking line card with a bridge device used to connect the two network processor units (NPUs) to the front-end MAC device.

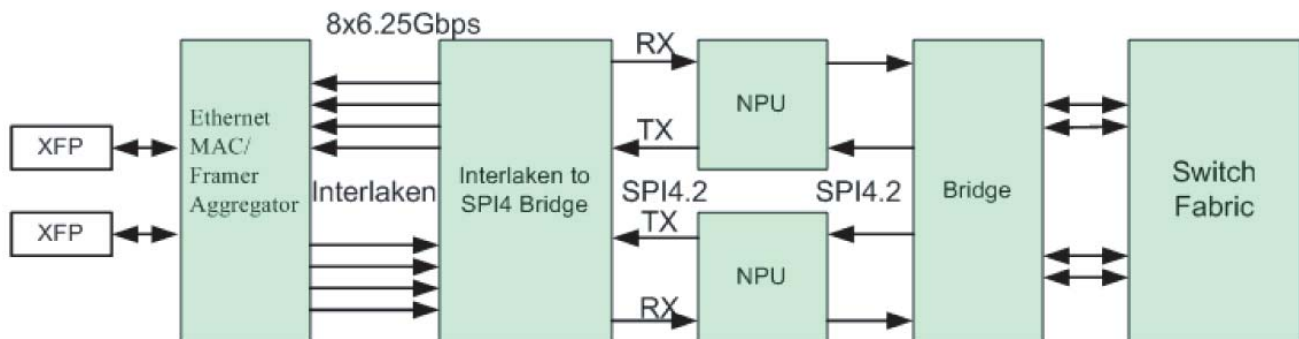


Figure 1. Block Diagram of a 20 Gbps Full Duplex Line Card

Altera's Stratix® GX and Stratix II GX field programmable gate array (FPGA) families with embedded multi-gigabit transceivers provide the ideal platform for developing bridging solutions to interconnect any two devices in networking equipment. Stratix II GX FPGAs are specifically architected to meet the full system demands of both current and future serial I/O based applications. Stratix II GX devices are built using the industry's fastest and highest-density FPGA architecture with up to 20 full-duplex high-performance multi-gigabit transceivers. These transceivers deliver excellent jitter performance across the full 600 Mbps to 6.375 Gbps range and when used with the multiple levels of dynamic pre-

emphasis and equalization circuits in the FPGA, provide a low risk design path for new system designs.

The remainder of this article provides a high level overview of the Interlaken protocol along with some of its features and advantages relative to older technologies. Additionally, the architecture and details of a 20 Gbps Interlaken to SPI4.2 bridge is discussed. The [bridge is comprised of a Stratix II GX FPGA](#) and uses [Sarance Technologies Interlaken IP Core \(IIPC\)](#) to create a 20 Gbps bridge. The IIPC is available today for both application specific integrated circuits (ASICs) and FPGAs, with the FPGA implementation specifically optimized to take advantage of the advanced structures available in the latest FPGAs. The IIPC is fully-compliant with the Interlaken protocol revision 1.1 specifications and provides a cost-effective, risk free, and quick time-to-market solution for system designers.

## **Interlaken Protocol Overview**

The Interlaken protocol is a scalable chip-to-chip interconnect technology designed to enable transmission speeds from 10 Gbps to 100 Gbps and beyond. Interlaken takes the best of existing solutions and builds a channelized protocol that operates over currently available serial link technologies.

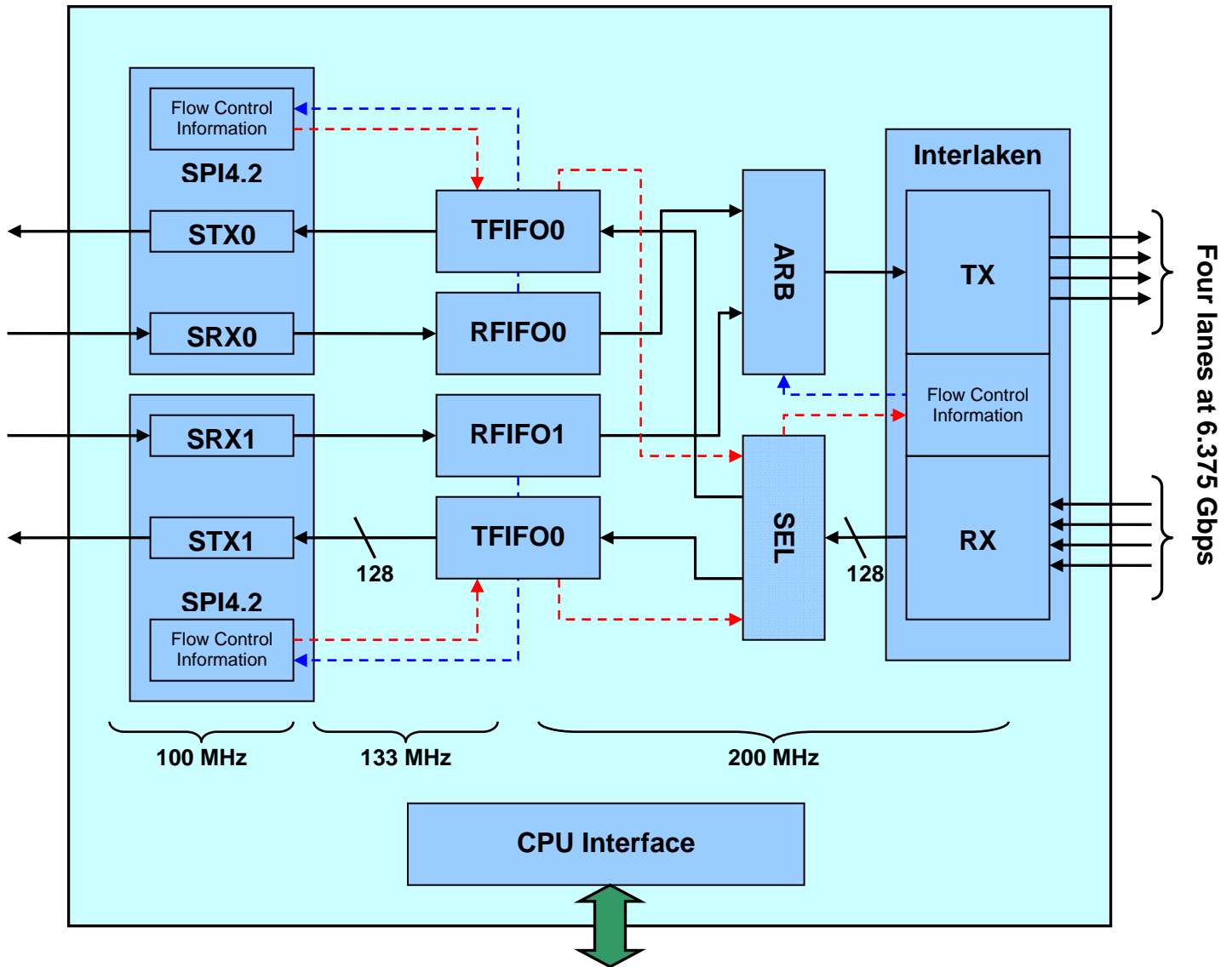
The channelized protocol is flexible enough to allow system designers to optimally designate different functions between multiple devices. For example, in a typical router, one device can be used to perform aggregation and classification before passing the packets to a second device that performs traffic management. With the channelized protocol of the Interlaken standard, the classification information is easily transmitted to the traffic manager without significant (if any) overhead.

Using a serial interface dramatically lowers the pin requirement for the chip-to-chip interface. Compared to the System Packet Interface level 4, phase 2 (SPI-4.2) protocol, Interlaken requires 90 percent fewer pins. In addition, the Interlaken protocol can be implemented using as many serial links as required to achieve the desired bandwidth. This scalable approach allows a simple and straight forward migration path for system designers to implement higher performance systems. There is no need to change the chip-to-chip interconnect technology in order to achieve higher bandwidths. The current Interlaken protocol implementation can be simply scaled by adding additional serial links, thus providing additional bandwidth.

The Interlaken protocol also improves the data integrity of the transmission link relative to other protocols. A 67/64 bit encoding scheme along with a self-synchronizing scrambler is used to maintain proper DC balance. Payload data integrity is monitored using a CRC24 mechanism and each serial link's integrity can be monitored using a CRC32 algorithm.

## **Architecture of a 2:1 Bridge**

Using Altera's POS-PHY Level 4 MegaCore functions and IIPC, a SPI-4.2 to Interlaken bridge can be easily constructed. In the following example, the bridge is used to connect two SPI-4.2 interfaces, each transferring 10 Gbps of data, to one Interlaken interface that transfers 20 Gbps of data (this is a 2:1 bridge). The block diagram of the bridge is shown in Figure 2.



**Figure 2. Block Diagram**

The bridge receives packets from two POS-PHY receivers, SRX0 and SRX1, and forwards them to the Interlaken transmitter, TX. The bridge also receives packets from the Interlaken receiver, RX, and forwards these to the appropriate POS-PHY transmitter, STX0 or STX1. The design uses an IIPC with a local bus of 128-bits, clocked at 200 MHz, and four high-speed SERDES lanes at 6.375 Gbps. The POS-PHY interfaces have data paths equal to 128-bits and the trefclk and rdint\_clk inputs are set to 100 MHz. The Atlantic interfaces of both SPI4.2 cores are clock at 133 MHz. The IIPC and the POS-PHY interfaces are connected via domain-crossing FIFOs.

The bridge is implemented in a Stratix II GX 60E device and the resource utilization is provided in Table 1.

Block	ALUTs	Logic Registers	Memory Blocks		Comments
			M512	M4K	
Interlaken	7970	4756	1	39	4 lanes @ 6.375 Gbps
SPI-4.2	6734	8974	6	76	Total for both SPI-4.2 Interfaces
Internal logic	5150	3760	15	56	Parametrizable Memory Utilization
<b>TOTAL</b>	<b>19854</b>	<b>17490</b>	<b>22</b>	<b>171</b>	

**Table 1. Device Resource Utilization for 2:1 Bridge**

Even though not specifically discussed in this article, many networking applications require a 1:1 bridge. That is, a bridge for connecting a single SPI-4.2 port to a two-lane Interlaken port. The 1:1 bridge can be implemented in a Stratix II GX 30C device using the same design guidelines as the 2:1 bridge. The resource utilization of the 1:1 bridge is provided in Table 2.

Block	ALUTs	Logic Registers	Memory Blocks		Comments
			M512	M4K	
Interlaken	4138	2871	1	21	2 lanes @ 6.375 Gbps
SPI-4.2	3367	4487	3	38	Single SPI-4.2 interface
Internal logic	3120	1880	10	30	Parametrizable Memory Utilization
<b>TOTAL</b>	<b>10625</b>	<b>9238</b>	<b>14</b>	<b>89</b>	

**Table 2. Device Resource Utilization for 2:1 Bridge**

It should be noted from Table 1 and Table 2 that the resource and memory utilization of the Interlaken block is *less* than the resource and memory utilization of the SPI-4.2 blocks for the same bandwidth. The IIPC is a highly efficient implementation of the Interlaken protocol and allows optimum design of networking systems.

### Technical Details of the 2:1 Bridge

Like SPI-4.2, the Interlaken protocol provides for channelized communications of packets. For this bridge, packets received via SRX0 will be transmitted on Interlaken channel 0 and packets received via SRX1 will be transmitted on Interlaken channel 1. Likewise, packets received by the Interlaken RX with a channel identifier of 0 will be forwarded to STX0 and packets received with a channel identifier of 1 will be forwarded to STX1.

Packets transferred via the Interlaken protocol are segmented into bursts. The size of these bursts is based on two parameters: BurstMax and BurstMin. For this example, segmentation will only depend on a BurstMax of 256 bytes. Packets transmitted will be segmented into 256 bytes segments except for the last segment that may be less than 256 bytes. This is not the optimal scheduling algorithm described in the Interlaken specification, but will suffice for this example.

Given the clock frequencies specified in Figure 2, the data rate on the Interlaken protocol is fast enough to transmit all the data received from SRX0 and SRX1. Therefore, there is no need for flow-control in the path from SRX0 and SRX1 to TX. However, the rate of the data received on the

Interlaken port (RX) can be faster than the maximum transmission rate of STX0 and STX1. This path requires flow-control as described below for proper operation.

The SPI-4.2 cores are configured such that packets received by SRX0 and SRX1 are written into their respective FIFOs: RFIFO0 and RFIFO1. The arbiter, ARB, selects which FIFO will be read. It alternates between RFIFO0 and RFIFO1 depending on which FIFO has 256 bytes of data. The arbiter switches when 256 bytes have been forwarded or has detected an End Of Packet (EOP). In addition, the ARB may stop packet transmission for one or both SPI-4.2 channels if the flow control information being received by the Interlaken interface is set to XOFF.

The RX output of the Interlaken core is connected to the two FIFOs crossing data to the SPI-4.2 transmitters: TFIFO0 and TFIFO1. The SEL block selects which SPI-4.2 interface to forward the packet to. The decision is based on which channel ID is received by the Interlaken RX block as described earlier.

The Interlaken protocol uses simple XOFF/XOFF protocol for in-band or out-of-band flow-control. Sarance's IIPC provides a separate flow-control input and output for each channel. In this example, when TFIFO0 is greater than half-full, the flow-control input for channel 0 becomes a value of 0 (i.e. XOFF). When TFIFO0 is less than half-full, the flow-control input for channel 0 is a value of 1 (i.e. XON). The flow-control input for channel 1 operates the same way with TFIFO1. It is the function of the (Interlaken protocol) sender to monitor this flow-control information and stop transmission of data as necessary.

## **Design Considerations**

There are several factors to consider when implementing the bridge. First, sufficient memory resources must be allocated for the clock domain crossing FIFOs to ensure traffic is transmitted without any interruptions. For the bridge described in this article, the memory requirements for the SPI-4.2 to Interlaken direction are relatively low as the ARB block only arbitrates between two SPI-4.2 interfaces. However, for the Interlaken to SPI-4.2 direction, if many packets are received for the same SPI-4.2 interface, the corresponding TFIFO may fill up. This is because on the Interlaken protocol receiving data at twice the rate of the individual SPI-4.2 interfaces. To avoid filling up the TFIFOs too often, as much memory as practical should be allocated for the TFIFOs.

To provide enough bandwidth to support 20 Gbps of Ethernet traffic, the SPI-4.2 interfaces and the Interlaken protocol must be clocked at a rate fast enough to ensure the required throughput is maintained for all possible packet sizes. In this example, the clock frequencies are chosen to support the worst case packet size of 65 bytes.

While SPI-4.2 has a fixed I/O definition, the Interlaken protocol allows designers to select the number and rate of the serial lanes. This bridge uses four serial lanes running at 6.375 Gbps each, for a total interface bit rate of 25.5 Gbps. When the BurstMax parameter is set to 256 bytes, the described bridge is capable of supporting 20 Gbps of Ethernet traffic.

## **Scalability**

With the FPGA technology available today, additional sophistication can be easily added to the bridge to improve the features. The bridge can be scaled in many different ways, such as:

- Increasing the throughput of the bridge
- Increasing the number channels per each SPI-4.2 interface
- Implementing a more sophisticated scheduling algorithm for the ARB and SEL blocks

Increasing the throughput of the bridge requires adding more SPI-4.2 interfaces and increasing the number of serial lanes for the Interlaken interface. This scenario serves as a good example to see the benefits of Interlaken: while doubling the SPI-4.2 throughput requires adding two more interfaces which in turn requires more I/O and result in more complicated ARB/SEL blocks. Increasing the Interlaken throughput simply requires adding four more serial lanes and doubling the internal bus size to 256 bits.

The analysis for increasing the number of logical channels and implementing more sophisticated algorithms for the ARB and SEL blocks is beyond the scope of this article. For more information contact Sarance Technologies ([www.sarance.com](http://www.sarance.com)).

## **Conclusions**

The Interlaken protocol eliminates the cost and performance barriers of existing interconnect standards by taking advantage of serial technology to build higher-performance networking equipment. This protocol is the future of high-speed, chip-to-chip interconnect technology for packetized interfaces. As an increased number of ASSPs become available with Interlaken interfaces, bridging devices are required to connect the new ASSPs with legacy devices. Implementing the functionality of a bridge device with two SPI-4.2 interfaces and one Interlaken interface using Altera's Stratix II GX FPGA and Sarance's Interlaken IP provides an easily-implemented solution.

## **REFERENCES**

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