SARANCE TECHNOLOGIES

DDR2 SDRAM Packet Buffer

INTRODUCTION

To provide emerging services like triple play on IP networks, data communication OEMs are being asked to incorporate advanced traffic management capabilities into their products. Traffic management is the act of identifying a particular data flow and imposing some type of transmission control onto that flow. One of the critical components of a traffic management solution is the packet buffer that is used to store the packet contents while the flow identification and transmission control processing is performed. To achieve packet rates at 10 Gbps or beyond, very high bandwidth to the packet buffer memory is required. To address the high bandwidth requirement, specialty memories like RLDRAM, FCRAM, and QDRII SRAM have been developed and are commercially available. The issue with these memory technologies is that they come at a very high price per bit, and in the case of RLDRAM and FCRAM, pose serious security of supply issues to the networking OEM.

To address the need for a high bandwidth yet cost effective packet buffering solution, Sarance Technologies' has developed and implemented a packet buffer that is based on DDR2 SDRAM devices. DDR2 SDRAM is widely used, and provides a cost effective alternative to other memory technologies, without suffering from any security of supply issues.

PACKET BUFFER ARCHITECTURE

The DDR2 Packet Buffer has been implemented as a scalable core to enable reuse among a wide range of application performance targets. Each core connects to a single DDR2 SDRAM device, and has sufficient memory bandwidth to support a worst case packet rate of 2.5 Gbps. At the heart of the packet buffer core is an address manager that is designed to efficiently use the DDR2 bus for maximum packet throughput. It assigns a user supplied data word to the SDRAM and returns a pointer that can then be used to access the same data at a later time. Figure 1 shows the block diagram of a single packet buffer core.

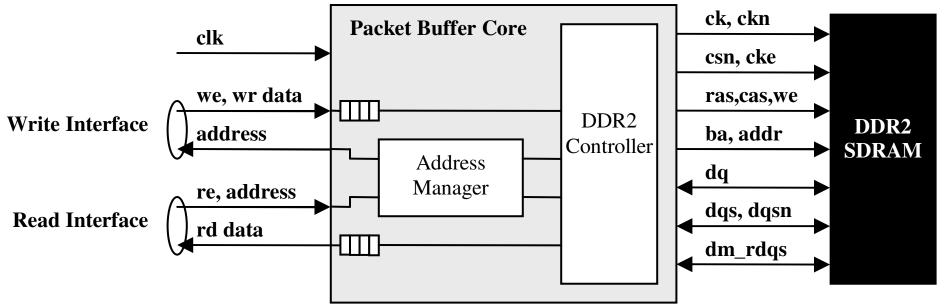

Figure 1. DDR2 Packet Buffer Module Block Diagram

The packet buffer core has been designed to support worst case symmetric data flow, wherein data is read from the buffer at the same rate that it is written to. It can be customized for asymmetric data flows (such as oversubscription applications), thereby further improving the actual packet throughput.

KEY FEATURES

- Each core supports 2.5 Gbps memory throughput
- Implemented using 266.7 MHz DDR2 SDRAMs
- Cores can be cascaded to support 5 Gbps or 10 Gbps applications
- Easily customizable for asymmetric applications

PERFORMANCE

The performance of the packet buffer is measured by its packet throughput, latency, and capacity. This section outlines the worst case packet throughput and the best case latency. Generally, latency and throughput can be traded off against one another to allow tuning to specific system requirements.

The throughput of the packet buffer, which varies as a function of packet length, is shown in Figure 2. The classic saw tooth performance curve comes about because the packet buffer core is configured to use the DDR2 SDRAM in burst of 8 mode. As such, the minimum word size of a write transaction to the core is 128 bits. This finite granularity, along with read and write turnaround times, defines the worst case throughput of the packet buffer. Note that this performance curve has been generated by targeting the lowest possible latency and assuming symmetrical writes and reads. By allowing higher write to read latency, or by allowing asymmetrical access, performance can be further improved.

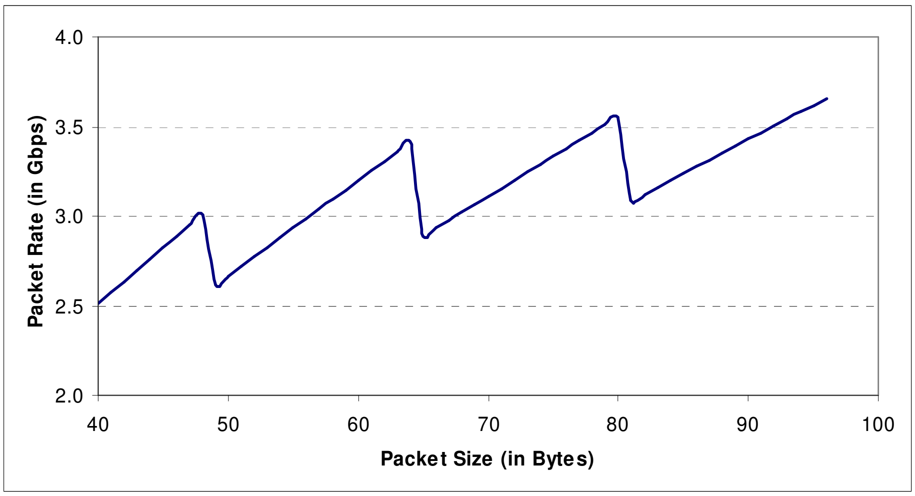

Figure 2. Packet Throughput as a Function of Packet Size

The latency of the packet buffer is defined as the time between starting a write of a packet to the packet buffer, and having the packet available for reading from the packet buffer. The best case latency for a 64 Byte packet is 165 ns.

Capacity is proportional to the size of the DDR2 SDRAM device used in the packet buffer. It also depends on the average size of the packets, as larger packets can be packed more densely than smaller packets. For a 256MB DDR2 SDRAM, and a throughput target of 2.5 Gbps, the packet buffer provides a worst case capacity of 25 ms of data.

AVAILABILITY

The Packet Buffer is available for licensing for implementation in an FPGA or ASIC, and can be purchased as either a targeted FPGA netlist or as generic Register Transfer Level (RTL) Verilog source code. Both options come with a test bench and detailed users manual.

Sarance Technologies also provides a broad range of FPGA design services to help customize IP to a specific requirement or to accelerate time to market of complex FPGA designs.

For more details on licensing or customizing the packet buffer to a specific requirement, or on general design services, please contact Sarance Technologies Inc at customers@sarance.com.

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