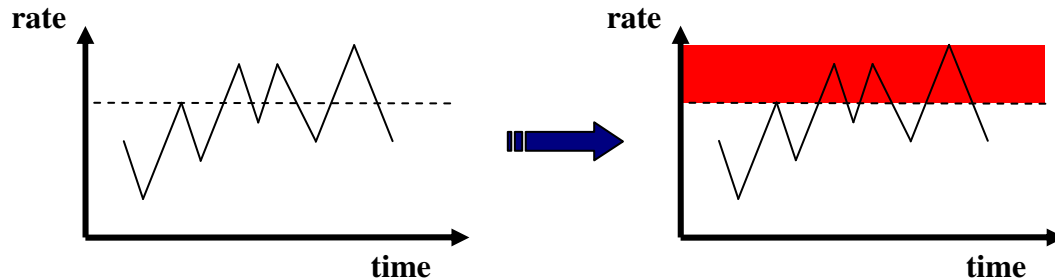


# SARANCE TECHNOLOGIES

## Intellectual Property Product Brief Traffic Policer

Traffic policing controls the maximum rate of traffic of a particular IP packet stream. The maximum rate of traffic is controlled by a token bucket algorithm that meters the packet stream and marks the traffic as green, yellow or red. The user can then apply a packet handling action based on the marking of the packets. Marking is based on a number of user configurable parameters, including committed information rate, committed burst size, excess burst size, peak information rate, and peak burst rate.



**Figure 1. Marking of packets that exceed some predetermined data rate**

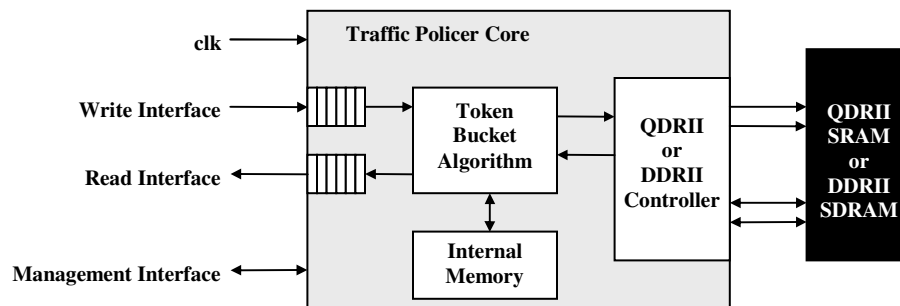
Sarance's Traffic Policing algorithm implements policing as described by the IETF RFCs 2697 and 2698.

RFC2697 describes a single rate, three color (SrTCM) marker based on a Committed Information Rate (CIR), and two associated burst sizes: Committed Burst Size (CBS), and Excess Burst Size (EBS). A packet is marked green if it doesn't exceed the CBS, yellow if it lies between the CBS and EBS, and red if it exceeds the EBS.

RFC2698 describes a two rate, three color (TrTCM) marker based on a Committed Information Rate (CIR), a Peak Information Rate (PIR), and two associated burst sizes: Committed Burst Size (CBS), and Peak Burst Size (PBS). A packet is marked red if it exceeds the PIR; otherwise it is marked yellow if it exceeds the CIR and green if it does not exceed the CIR.

### POLICER CORE ARCHITECTURE

The traffic policer core operates on the flow identifier associated with a particular packet. Based on the rate parameter assigned to that particular flow, the token bucket algorithm returns a colored marking and/or remarks the DSCP of the packet. The packet core utilizes internal memory to utilize small numbers of flows (< 8K) and has an external memory port to support up to 128K flows.



**Figure 2. Traffic Policer Block Diagram**

**IMPLEMENTATION**

Sarance Technologies’ traffic policing algorithm supports over 128k packet flow identifiers, each of which has independently configurable state parameters. The algorithm is targeted for implementation in an FPGA, with the token buckets stored in external memory or internal memory. The number of required flows determines the amount of internal and external memory required. The following table shows the internal memory allocation for a Stratix2 FPGA.

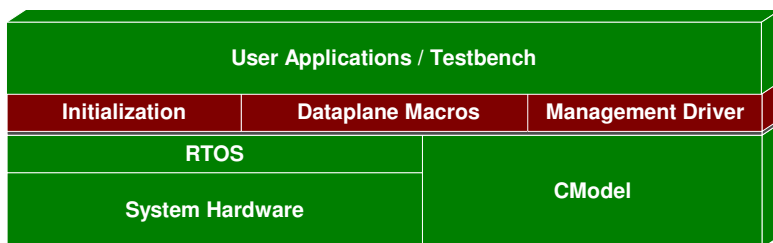
Eight M4K Memory Blocks	Holds 128 Flow state tables
One M-RAM Memory Block	Holds 2K Flow state tables

The state of each individual stream has a set of configuration parameters, and a current state that is stored in memory. The following table shows the information that is stored for each individual stream. All of the information stored must be retrieved and updated for each incident packet. The amount of memory accesses required is thus high which makes the policing function an ideal candidate to offload from a packet processor.

Field	Width	Description
CIR	12	Committed Information Rate (CIR)
CBS	10	Committed Burst Size (CBS).
PIR	12	Peak Information Rate (PIR)
PBS	10	Peak Burst Size (PBS)
CBSBurst	35	Current CBS state
PBSBurst	35	Current PBS state
LastPktTime	24	Last time the flow states (i.e., CBSBurst and PBSBurst) were updated
GreenCount	32	Green packets or bytes
YellowCount	32	Yellow packets or bytes
RedCount	32	Red packets or bytes
<b>Total</b>	<b>234</b>	

**SOFTWARE DEVELOPMENT KIT**

Sarance provides a complete Software Development Kit (SDK) that facilitates the design of the traffic policer into a packet processing system. In addition to control and data plane drivers, the SDK provides a C/C++ model that can be used to model the performance of the search engine in a software simulation of the processing system.



**AVAILABILITY**

The traffic policing algorithm is available for licensing for implementation in an FPGA or ASIC, and comes with a complete software development kit. Sarance Technologies also provides a broad range of FPGA design services to help customize IP to a specific requirement or to accelerate time to market of complex FPGA designs.

For more details on licensing or customizing the traffic policer to a specific requirement, or on general design services, please contact Sarance Technologies Inc at [customers@sarance.com](mailto:customers@sarance.com).

Tel: 613-792-4050 <a href="mailto:customers@sarance.com">customers@sarance.com</a>	<b>Sarance Technologies Inc.</b> <b><a href="http://www.sarance.com">www.sarance.com</a></b>	880 Lady Ellen Place Ottawa ON K1Z 5L9
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